PATENT APPLICATION
Docket No. 4591-350
Client No. IE10077-US-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re application of: | Hyun-Ho Kim | Conf. No. | 1807 |
| Serial No. | 10/621,851 | Examiner: | Tsai, H Jey |
| Filed: | July 16, 2004 | Art Unit: | 2812 |
| For: | FERROELECTRIC MEMORY DEVICE AND METHOD OF FABRICATING THE SAME | | |

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**TRANSMITTAL LETTER**

Enclosed for filing in the above-referenced application are the following:

- ☒ Applicant's Comment's on Examiner's Statement of Response for Allowance
- ☒ Publication and Issue Fee
- ☒ In connection with issuance of a patent:
  - ☐ Supplemental Declaration ☒ PTO Form 85B
- ☒ PTO Form 2038 authorizing credit card payment of $1630.00, issue fee ($1330.00) and publication fee ($300.00) is enclosed.
- ☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

**Customer No. 20575**

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Alan T. McCollom
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
Date: May 3, 2004

Adrienne Chocholak

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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## APPLICANT'S COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

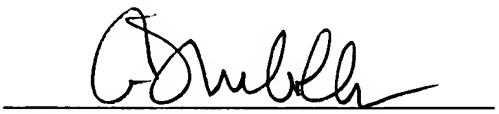
Applicant submits that the prior art alone or in combination does not teach a method of fabricating a ferroelectric memory device comprising the steps of: forming first and second switching elements on a semiconductor substrate; forming an interlayer insulating layer covering the first and second switching elements; forming first and second contact plugs in the interlayer insulating layer, the first and second contact plugs being coupled to the first and second switching elements, respectively; forming, on the interlayer insulating layer, capacitors where a lower electrode coupled to the first contact plug, a first ferroelectric layer, a middle electrode, a second ferroelectric layer, and an upper electrode are sequentially stacked; forming an insulating layer covering the capacitor, the second contact plug, and the interlayer insulating layer; and forming, in the insulating layer, an interconnection for connecting the second contact plug to the upper electrode, as recited in allowed claim 1. Applicant submits that the prior art alone or in combination does not teach a method of fabricating a ferroelectric memory device comprising the steps of: forming a switching element on a semiconductor substrate; forming an interlayer insulating layer covering the switching element; forming a contact plug coupled to the switching element in the interlayer insulating layer; forming, on the interlayer insulating layer, first and second capacitors comprising a lower electrode, a first ferroelectric layer, a middle electrode, a second ferroelectric layer, and an upper electrode; forming an insulating layer covering the first and

second capacitors, the contact plug, and the interlayer insulating layer; and forming an interconnection for connecting the contact plug to the middle electrode in the insulating layer, as recited in allowed claims 6. Applicant submits that the prior art alone or in combination doest not teach a method of fabricating a ferroelectric memory device comprising the steps of: forming a switching element on a semiconductor substrate; forming an interlayer insulating layer covering the switching element; forming a contact plug coupled to the switching element in the interlayer insulating layer; forming, on the interlayer insulating layer, first and second capacitors comprising a lower electrode coupled to the contact plug, a first ferroelectric layer, a middle electrode, a second ferroelectric layer, and an upper electrode sequentially stacked; forming an insulating layer covering the first and second capacitors and the interlayer insulating layer; and forming an interconnection for connecting the lower electrode to the upper electrode in the insulating layer, as recited in allowed claims 11.

**Customer No. 20575**

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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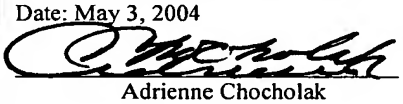

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